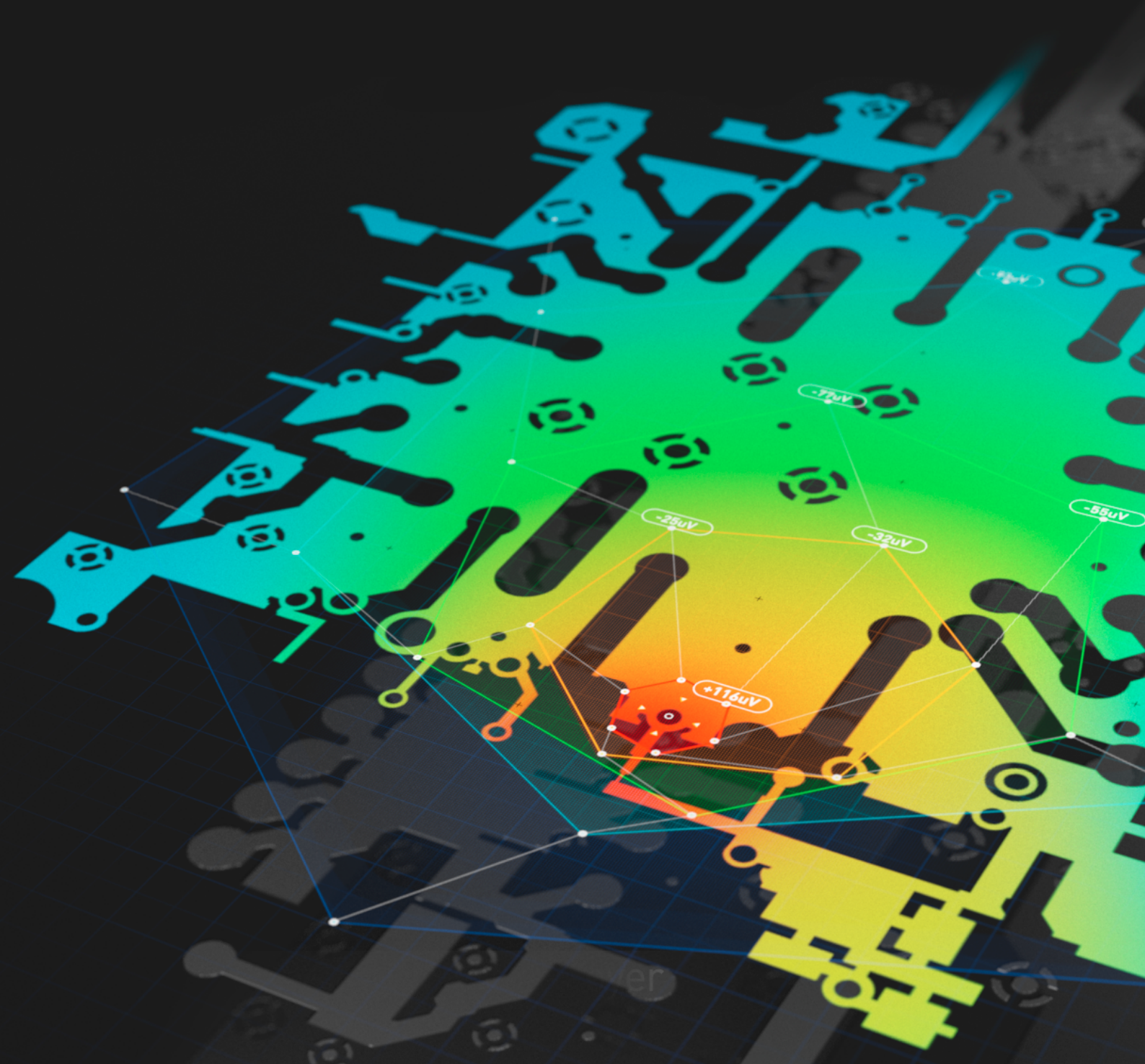


10 SYMPTOMS OF A BAD PDN



WHAT IS POWER INTEGRITY?

At face value, DC power integrity seems to be a simple enough topic -- you just need to make sure that every component on your PCB has the power (current and voltage) it needs when it needs it. But that's just on the surface. The new reality is a bit more complicated. When you start to work with fine-pitch device packages, the manufacturing constraints and power requirements of said devices are almost completely at odds with each other. Not only is it difficult to get the required current to all the power pins, but you are also working with multiple supply voltages. This means that, unless you want a high-layer-count PCB, you will have to get power to your devices through various split planes, and that's where the trouble begins.

You're going to have to plan and design a proper power distribution network, or PDN. For many designers, the PDN is a foreign and intimidating part of the PCB design process and rightly so because creating your actual PDN can be quite demanding, requiring specialized training and experience. On the other hand, optimizing the performance of your power distribution network isn't as complex. In fact, the fundamental goal of optimizing your PDN can be as straightforward as your PCB design process — provide enough current and voltage to every load to meet their operation requirements. Ensuring there's enough metal between each of the sources and their corresponding loads is the most critical aspect of the PCB in regards to PDN performance.

Now, power integrity is nothing new, it's actually a topic that's been around for a long time but only in recent years has it started to become a real concern. The main cause for this being miniaturization; our boards are getting smaller, a lot smaller. Wearables are a great example of this; with smartwatches we're putting a small computer on your wrist with wireless connectivity, a battery, and a screen all in such a small package. It's incredible!

This quest for smaller and smaller products has led to more dense components that draw higher currents all while requiring tighter power supply voltage tolerances. And we need to be able to properly power these components at all stages of operation.

WHAT'S THE PROBLEM?

The problem of power integrity is a simple one, components aren't getting the power they need, when they need it. You may wonder, is it really that difficult to solve? Just put down more copper, or add more vias. While adding more vias and copper may help, you can't always do so.

When it comes to copper, you may be tempted to dump as much as possible on your board to take care of any problems that may arise, whether it be thermal or voltage issues, but those days are gone – even server designs are becoming incredibly dense and board real estate is a valuable commodity that can't be wasted with overly conservative design practices. All metal dedicated to power delivery must be "necessary", we don't have the luxury of additional layers or board size. This is especially true today with IoT and wearables, and the form factors we have to conform to.

Adding only "necessary" copper isn't just to help curb your board cost and stay within budget, it's also for the functionality and reliability of the board. You may be wondering how having unused or unnecessary copper could hurt you, well think of this: copper poured haphazardly may result in copper islands and peninsulas that have been known to cause board failures. They do this by becoming antennas, radiating at their specific resonant frequencies. And since the conditions to reproduce these resonant frequencies are extremely difficult to achieve, it's almost impossible to troubleshoot, often inviting a board redesign.

Something else you should watch out for are excessive vias; excessive in number of vias and also in size. When adding vias, you don't just perforate your necessary copper planes, you're also taking away valuable real estate from your signal layers, making it more difficult to route your board and make sure the copper is balanced throughout. Once you do that you start playing a dangerous game, but then again that's part of the job, we need to find a balance.

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When looking for that balance you may be tempted to turn to IPC-2152. That's not a bad thing to do, but you shouldn't use IPC-2152 as the first and final resource. When looking at IPC-2152 you must realize that they're setting you up with minimums (width, thickness, etc...) for a worst case scenario. If you're able to adhere to the IPC standard and still fit in your enclosure then that's great, but not the best design practice. With IPC-2152 you're going to be over designing, adding too much copper that's too thick and too many vias that are too large.

IPC-2152 is a great tool to have at your disposal and should be well understood if you want to make the most efficient power delivery designs, but it shouldn't be blindly applied. Engineers who use IPC-2152 in a more thoughtful way alongside a power integrity tool can reduce their power distribution network area while still ensuring a safe design goes out for production.

SYMPTOMS

A bad PDN can show itself in many ways and for some the moment you try looking for these issues is the moment they can't easily be reproduced. You may have a power integrity issue if you experience any of these issues in your assemblies:

1. The CPU is resetting unexpectedly or when a high-utilization thread enters execution.
2. Memory devices keep failing their content retention/corruption tests.
3. Analog front-end circuits are randomly inaccurate or out of design specs.
4. CPU or FPGA devices fail catastrophically.
5. FPGA configurations are corrupted during powerup.
6. PCB vias go open circuit after a number of use cycles, or maybe even at first power on.
7. Production PCBs suffer blistering in common locations.
8. PCBs suffer delamination in common locations.
9. Trace or polygon neckdowns are fusing.
10. Laminate or solder mask material is discolored in some regions of the PCB.

These symptoms fall into two broad categories of DC power integrity problems. For example, items 1-5 are the more sinister misbehaviors caused by transient voltage drops across the board. Sometimes they can be fixed with better decoupling, but when you're talking DC, only adding more copper will really improve the design. Items 6-10 are more serious power integrity issues where current density regularly exceeds the safe limits for temperature rise. The board is suffering from localized heating, or copper is outright fusing.

There are some useful tools for avoiding these sorts of problems before prototype, such as the IPC-2152 conductor sizing charts mentioned earlier. I will say again that it's a great place to start your design but if you really want to produce an optimal design for today's products then you'll need to use an integrated power integrity tool while designing your PCB. Fortunately, tools exist for exactly that purpose. That way you can correct these problems before any prototype is built, saving you time, money, and possibly your job.